CLAIMS

1. (Currently amended) A data strobe circuit, comprising:

a first logic unit ~~capable of generating~~ to generate a pull up control signal responsive to first and second clock signals;

a second logic unit ~~capable of generating~~ to generate a pull down signal responsive to the first and second clock signals; and

a data strobe buffer ~~capable of generating~~ to generate a data strobe signal responsive to the pull up and pull down control signals, the data strobe signal including a preamble;

where the first logic unit is ~~capable of generating~~ to generate the preamble responsive to a first pulse of the first clock signal; and

where the data strobe signal is in a high impedance state responsive to a last pulse of the first clock signal.

2. (Original) The data strobe circuit of claim 1

where the data strobe signal is in a first logic level responsive to the pull up and pull down control signals that are, in turn, responsive to pulses other than the first and last pulse of the first clock signal; and

where the data strobe signal is in a second logic level responsive to the pull up and pull down control signals that are, in turn, responsive to the second clock signal.

3. (Original) The data strobe circuit of claim 1 where the second clock signal is ½ cycle out of phase from the first clock signal.

4. (Currently amended) The data strobe circuit of claim 1

where the first logic unit is ~~capable of receiving~~ to receive an even data control signal responsive to a read command; and

where the second logic unit is ~~capable of receiving~~ to receive an odd data control signal responsive to the read command.

5. (Currently amended) The data strobe circuit of claim 1 where the first logic unit includes:

a first logic gate ~~capable of generating~~ to generate a first output signal by logically manipulating an even data control signal and a logic high signal;

a second logic gate ~~capable of generating~~ to generate a second output signal by inverting the first output;

a first transmission gate ~~capable of providing~~ to provide the second output signal to a first output node responsive to the first clock signal; and

a second transmission gate ~~capable of providing~~ to provide a logic low signal to the first output node responsive to the second clock signal.

6. (Currently amended) The data strobe circuit of claim 5 where the second logic unit includes:

a third logic gate ~~capable of generating~~ to generate a third output signal by inverting the even data control signal;

a fourth logic gate ~~capable of generating~~ to generate a fourth output signal by logically manipulating the preamble and the third output signal;

a third transmission gate ~~capable of providing~~ to provide the fourth output signal to a second output node responsive to the first clock signal;

a fifth logic gate ~~capable of generating~~ to generate a sixth output signal by inverting an odd data control signal; and

a fourth transmission gate ~~capable of generating~~ to generate the sixth output signal to the second output node responsive to the second clock signal.

7. (Original) The data strobe circuit of claim 1 where the data strobe buffer comprises:

a pull up transistor operating responsive to the pull up control signal; and

a pull down transistor operating responsive to the pull down control signal.

8. (Cancelled)

9. (Currently amended) A ~~The~~ circuit ~~of claim 8~~, comprising:

a data strobe buffer to generate a data strobe signal responsive to pull up and pull down control signals;

a first latch to latch a pull up signal at a first node;

a second latch to latch a pull down signal at a second node;

a first logic circuit to generate the pull up signal responsive to an even data control signal and a preamble control signal; and

a second logic circuit to generate the pull down signal responsive to an odd data control signal;

where the first and second logic circuits operates responsive to first and second clock signals.

10. (Original) The circuit of claim 9 where the second clock signal is out of phase relative to the first clock signal.

11. (Currently amended) The circuit of claim ~~8~~ 9 where the data strobe buffer comprises:

a first inverter ~~capable of inverting~~ to invert the pull up signal;

a second inverter ~~capable of inverting~~ to invert the pull down signal;

a pull up transistor ~~capable of generating~~ to generate the data strobe signal responsive to the inverted pull up signal; and

a pull down transistor ~~capable of generating~~ to generate the data strobe signal responsive to the inverted pull down signal.

12. (Currently amended) The circuit of claim ~~8~~ 9

where the first latch includes a first inverter ~~capable of inverting~~ to invert a latched pull up signal; and

where the second latch includes a second inverter ~~capable of inverting~~ to invert a latched pull down signal.

13. (Currently amended) A ~~The~~ circuit ~~of claim 8~~, comprising:

a data strobe buffer to generate a data strobe signal responsive to pull up and pull down control signals;

a first latch to latch a pull up signal at a first node;

a second latch to latch a pull down signal at a second node;

a first logic circuit to generate the pull up signal responsive to an even data control signal and a preamble control signal; and

a second logic circuit to generate the pull down signal responsive to an odd data control signal;

where the first logic circuit comprises:

a logic gate ~~capable of logically manipulating~~ to logically manipulate the even data control signal with a logic high level signal;

an inverter ~~capable of inverting~~ to invert an output of the logic gate;

a first transmission gate ~~capable of providing~~ to provide an output of the inverter as the pull up signal responsive to a first clock signal; and

a second transmission gate ~~capable of providing~~ to provide a logic low level signal as the pull up signal responsive to the second clock signal.

14. (Currently amended) A ~~The~~ circuit ~~of claim 8~~, comprising:

a data strobe buffer to generate a data strobe signal responsive to pull up and pull down control signals;

a first latch to latch a pull up signal at a first node;

a second latch to latch a pull down signal at a second node;

a first logic circuit to generate the pull up signal responsive to an even data control signal and a preamble control signal; and

a second logic circuit to generate the pull down signal responsive to an odd data control signal;

where the second logic circuit comprises:

a first inverter ~~capable of inverting~~ to invert the even data control signal;

a logic gate ~~capable of logically manipulating~~ to logically manipulate an output of the first inverter with the preamble control signal;

a first transmission gate ~~capable of providing~~ to provide an output of the logic gate as the pull down signal responsive to the first clock signal;

a second inverter ~~capable of inverting~~ to invert the odd data control signal; and

a second transmission gate ~~capable of providing~~ to provide an output of the second inverter as the pull down signal responsive to the second clock signal.

15. (Currently amended) The circuit of claim ~~8~~ 9 where the even and odd data and preamble control signals operate responsive to a read command.